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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,542	06/25/2003	Jiun-Jye Chang	10112281	4078

7590 01/20/2004

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,542	CHANG ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-23* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The disclosure is objected to because of the following informalities: page 7 line 8 of the DETAILED DESCRIPTION OF THE INVENTION, where it is stated that in Fig. 2C, the photoresist pattern 240 is removed, however Fig. 2C does not disclose a removed photoresist pattern but Fig. 2D shows a removed photoresist pattern therefore it would imply that Fig. 2D shows the removed pattern 240. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. US Patent 6,548,331 view of conventional prior art.

4. Lee discloses the semiconductor method substantially as claimed. See **Figs. 1A-8E** where Lee teaches a method of forming a thin film transistor device, comprising the steps of:

providing a substrate **20**;

using a first reticle and forming a semiconductor island **21** on the substrate;

forming an oxide layer **22** on the semiconductor island;

forming a metal layer **23** on the oxide layer;

using a second reticle and forming a pattern **24** on part of the metal layer;

using the pattern **24** as a mask and isotropically etching part of the oxide layer to form a gate and gate dielectric layer, wherein the pattern is wider than the gate and gate dielectric layer but narrower than the semiconductor island;

using the pattern as a mask and performing a heavy doping ion implantation on the semiconductor island to form a source/drain region **21S/21D** in part of the semiconductor island;

removing the pattern; and

using the gate **23** as a mask and performing a light doping ion implantation on the semiconductor island to form a lightly doped drain (LDD) region in part of the semiconductor island.

However, Lee fails the step of using the photoresist pattern. See **col. 3 lines 25-40** where Lee teaches that a gate insulation layer, lower gate electrode, and an upper gate electrode, are sequentially formed on the active layer in order to form a lightly doped drain (LDD) region. Then an ion doping process is performed in two stages. In the first ion doping stage, a high-density doping is performed for form a source region and a drain region then as shown in Fig. 2D the upper gate electrode is removed and a low-density doping is performed to form lightly doped drain region (LDD). In view of Lee, it would have been obvious to one of ordinary skill in the art to incorporate a photoresist pattern into the Lee semiconductor method because since the upper gate electrode is removed to form a (LDD) region it would imply that any material that can be used as a sacrificial layer would apply since the ion doping process is performed in two stages.

5. Pertaining to claim 2, Lee teaches the method according to claim 1, wherein the substrate is a glass substrate.

6. Pertaining to claim 3, Lee teaches the method according to claim 1, wherein the semiconductor island is a polysilicon layer.

7. Pertaining to claim 4, Lee teaches the method according to claim 1, wherein the oxide layer is SiO_2 layer.

8. Pertaining to claim 5, Lee teaches the method according to claim1, wherein the metal layer is an Al, Ti, Ta, Cr, Mo, MoW or alloy of the above layer.

Allowable Subject Matter

9. Claims 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: Applicant's dependent claim 6 indicates allowable subject matter because none teach or render obvious a method according to claim 1, wherein the method of isotropically etching part of the metal layer and the oxide layer comprises wherein the second etching rate is greater than the first etching rate in order to make the width of the gate dielectric layer smaller than the width of the gate.

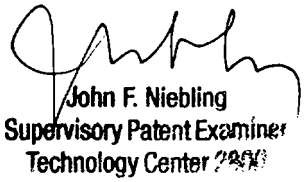
11. Claims 11-23 are allowed.

12. The following is an examiner's statement of reasons for allowance: Applicant's independent claim 11 is allowed over the prior art of record because none teach or render obvious a method of forming a thin film transistor device on a color filter, comprising the steps of forming a first buffer layer on the color filter and the metal layer and using a second reticle and forming a semiconductor island on the first buffer layer in the active area. See **Yamazaki et**

al. Patent Application Publication **2002/0024051** where teaches the semiconductor method of forming a thin film transistor device on a color filter however, fails the step of forming a buffer layer on the color filter and then forming a semiconductor island on the buffer layer in the active area.

13. All dependent claims are also rendered allowable.

14. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."



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